Abstract

Master's attestation work on:

"Methods of designing ADC"

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The Relevance

Analog-to-digital conversion is one of the most powerful technologies that shape science and engineering.

The successful conversion of analog signals to digital is not possible without designing appropriate devices.

With the transition to new manufacturing and design technology requirements for the IC devices to the analog-digital conversion architecture, resolution, power consumption and speed increases.

Therefore the methods of designing ADC is an important and relevant topic.

The Purpose

The purpose of this diploma is to investigate the design of 14–bit resolution ADC with sampling frequency 2 MHz in 0.13 um technology.

Problems that are solved

To achieve this goal in this paper the following problems were solved:

- analysis of methods of designing ADC;
- ADC behavioral modeling and parameters estimation;
- Carrying out the calculations of circuit.

The achieved results

Upon reaching the result in solving problems in goal, the author defends:

- Simulation results of modeling mismatch effect;
- Simulation results of modeling comparator offset voltage ;
- Result of methods of designing ADC analysis;
- Result of estimated calculation for ADC in SG013S IHP technology.

Scientific novelty

Scientific novelty of the work are the results of the investigation of schematic solutions for designing 14-bit ADC in technology SG013S IHP

The practical value

The practical value of the work is in the results of analysis of modern methods of designing ADC, development of program for modeling in MATLAB environment and behavioral model realized in Verilog-a language in Cadence environment for 14-bit successive approximation ADC, and the achieved estimation results and schematic solutions for particular blocks.

Conclusion:

1. Analysis of methods of designing ADC was done.
2. SAR architecture was chosen as most appropriate architecture to meet given specification.
3. Analysis of SAR ADC architectures was done.
4. Development of program for modeling successive-approximation analog-to-digital conversion in MATLAB was done.
5. Development of program for estimation of dynamic and static parameters in MATLAB was done.
6. Analysis of non–ideal effects in SAR ADC was done.

7. Modeling of mismatch, input referred dc offset and settling time effects was done.
8. Simulation of modeling mismatch effect shows that for SG013S IHP technology it is possible to get DNL ≤ 0.5 LSB, INL < 0.5 LSB, THD = -95.07 dB, SFDR = 85.75 dB, SINAD =84.84 dB, ENOB = 13.8 bit with probability 99.7%.
9. Simulation of modeling comparator offset voltage effect shows that for SG013S IHP technology with 3.2 mV input referred dc offset it is possible to get THD = -84.33 dB, SFDR = 76.10 dB, SINAD =74.95 dB, ENOB = 12.16 bit with probability 99.7%.
10. Simulation of modeling settling time effect shows that for SG013S IHP technology with 2.1 ns time constant it is possible to get SFDR = 83.97 dB, SINAD =83.7 dB, ENOB = 13.61 bit with probability 99.7%.
11. Verilog–a behavioral model of 14-bit differential charge–redistribution SAR ADC with monotonic switching procedure was developed.
12. Simulation of proposed high-speed comparator with resolution 40uV, clock frequency 100 MHz, supply voltage 1.2 V in SG013S IHP technology was done.
13. Analysis of more than 45 scientific sources up to 2011 year in the field of analog-to-digital conversion has been conducted.

Results of investigation have been published at the International conference on system analysis and information technologies.

The investigation was carried out for IHP - Innovations for High Performance Microelectronics company.

The work contains: 100 pages, 46 pictures, 3 tables, 45 sources

Key Words: ADC, SAR, non-ideal effects modeling, mathematical model, behavioral model.